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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

TRAN, TAN N

ART UNIT PAPER NUMBER

2826

DATE MAILED: 12 20 2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/007,833

Applicant(s)

AVERY ET AL.

Examiner

TAN N TRAN

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on amendment filed on 10/08/02.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-31 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) 24-29 and 31 is/are allowed.
- 6) ☒ Claim(s) 1-23 and 30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 5,6,18,30 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification does not disclose the bases of the first and second transistors have base widths less than 4.0 microns as recited in claim 5.

The specification does not disclose the bases of the first and second transistors have base widths in a range of 0.6 to 0.8, as recited in claim 6.

The specification does not disclose the respective base widths between the P+ doped region and the junction, and between the at least one N+doped region and the junction are less than 4.0 microns as recited in claim 18.

The specification does not disclose the respective base widths between the N+ doped region and the junction, and between the at least one P+doped region and the junction are less than 4.0 microns as recited in claim 30.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention

Claims 9,10,12,13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 9,12, lines 1,2, "the source and drain of the MOSFET" lacks of antecedent basis.

In claims 10,13, line 1, "the gate of the MOSFET" lacks of antecedent basis:

line 2, "the source of the MOSFET" lacks of antecedent basis.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1,2 are rejected under 35 U.S.C. 102(e) as being anticipated by Russ (2002 0041007).

With regard to claim 1, Russ discloses an electrostatic discharge protection circuit comprising a silicon controlled rectifier 102(202) having an anode 122(222) coupled to the protected circuitry and a cathode 124(224) coupled to ground, the N+ cathode 124(224) having at least one first high doped region: at least one trigger-tap 320(322), disposed proximate to the at least one high-doped region and an external on-chip triggering device 205 coupled to the trigger-tap 322 and protected circuitry through the SCR (202). (Note lines 2.3, paragraph 0005, page 1: lines 1.2, paragraph 0028, page 3:lines 14-16, paragraph 0035, and lines 4-6, paragraph 0036, page 4 figs. 1-5 of Russ).

With regard to claim 2, Russ discloses a lateral shunt resistor R_{p1} coupled between the cathode 124 and the external triggering device 205. (Note figs. 2-5 of Russ).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3,5-7,15,16,18,19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Russ (2002/0041007).

With regard to claim 15, Russ discloses a SCR comprising a substrate 302; a N-well 308₁ and an adjacent P-well 306₁ formed in the substrate 302 and defining a junction therebetween; at

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least on N + doped region 310₁₋₁ in the p-well 306₁ and coupled to ground 330_c; a P+ doped region 312₁₋₁ in the N-well 308₁ and coupled to a pad 132 of the protected circuitry; at least one p+ doped trigger-tap 322 disposed proximate to the at least one N+doped region in the P-well 306₁ and an external triggering device coupled to the SCR wherein one terminal is coupled to the trigger tap. (Note lines 2.3, paragraph 0005, page 1; lines 1.2, paragraph 0028, page 3; lines 14-16, paragraph 0035, and lines 4-6, paragraph 0036, page 4 figs. 1-4 of Russ). Russ discloses all the claimed subject matter except another terminal of the triggering device is connected to the pad. However, it would have been obvious to one of ordinary skill in the art to form another terminal of the triggering device is connected to the pad in order to turn on the SCR so that the circuitry can be protected from ESD. Note Note figs. 1A, 1B of Applicant's prior art is cited to support for the well know position.

With regard to claim 16, Russ discloses the terminal of the triggering device having trigger gate 105 is coupled to ground 124 via a resistor Rp1. (Note fig. 1 of Russ).

With regard to claim 19, Russ discloses a P-well-tie 322₁ is coupled to the Pwell and grounded. (Note figs. 2 and 5 of Russ).

With regard to claims 3,7, Russ discloses the SCR comprises a first bipolar transistor (QN1) and a second bipolar transistor (QN2); the first bipolar transistor (QN1) having the at least one first high doped region 310₁₋₁ serving as an emitter and forming the cathode, a first low doped region 306₁ coextensively forming a base of the first bipolar transistor (QN1) and a collector of the second bipolar transistor (QN2), a second low doped region 308₁ coextensively forming a base of the second bipolar transistor (QN2) and a collector of the first bipolar

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transistor (QN1), and a second high doped region 312₁₋₁ serving as an emitter of the second bipolar transistor (QN2) and forming the anode. (Note fig. 4 of Russ).

With regard to claims 5,6,18, APA and Russ disclose all claimed invention as in claim 3, except the bases of the first and second transistors have base widths in a range of 0.6 to 0.8 or less than 4.0 microns. However, although APA and Russ do not teach exact the base width range of transistor as that claimed by Applicant, the base width range differences are considered obvious design choices and are not patentable unless unobvious or expected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note in re Leshin, 125 USPQ 416.

Claims 4,8-14,17,20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Russ (2002/0041007) in view of Polgreen et al. (5,465,189).

With regard to claims 4,14,17,23, Russ does not disclose a surface area between the respective first and second high-doped regions of the first and second bipolar transistors are blocked from shallow isolation.

However, Polgreen et al. discloses a surface area over a non high-doped region (p_2, n_1) and between the respective first and second high-doped regions (n_2^+, p_1^+) of the first and second bipolar transistors are blocked from shallow isolation 6. (Note figs. 1 a, 14 of Polgreen et al.).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Russ's device having a surface area that is between the respective first and second high-doped regions of the first and second bipolar transistors is blocked from shallow isolation such as

taught by Polgreen et al. in order to prevent the short circuit between the anode electrode and the cathode electrode of SCR.

With regard to claims 8,20, Russ do not disclose the triggering device is MOSFET transistor selected from the group consisting of a NMOS, a NMOS provided with drain-bulk-gate coupling, a NMOS in an isolated p-well, at least two cascaded NMOS transistors, and a ballasted NMOS.

However, Polgreen et al. discloses the trigger device is a MOSFET transistor selected from the transistor group consisting of a NMOS. (Note Fig. 14, 16, 18 of Polgreen et al.).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Russ and APA's device having the trigger device is a MOSFET transistor selected from the transistor group consisting of a NMOS such as taught by Polgreen et al. in order to protect the IC circuitry from electrostatic discharges.

With regard to claims 9,12,21, Polgreen et al. discloses the source and drain of the MOSFET transistor are respectively coupled to the trigger-tap p+ type and to the protected circuitry. (Note Fig. 14, 16, 18 of Polgreen et al.).

With regard to claims 10,22, Polgreen et al. discloses the gate of the MOSFET is coupled to the source of the MOSFET transistor selected from the transistor group consisting of the NMOS. (Note fig. 18 of Polgreen et al.).

With regard to claim 11, Russ and Polgreen et al. disclose all the claimed subject matter except for the triggering device is a MOSFET transistor selected from the transistor group consisting of a PMOS. However, it would have been obvious to one of ordinary skill in the art to

form the triggering device of Polgreen et al. is a MOSFET transistor selected from the transistor group consisting of a PMOS, because NMOS can be replaced by PMOS.

With regard to claim 13, Polgreen et al. discloses the gate of the MOSFET is indirectly coupled to the source of the MOSFET transistor selected from the transistor group consisting of the NMOS. (Note fig. 18 of Polgreen et al.). It would have been obvious to one of ordinary skill in the art to replace the NMOS FET of Polgreen et al. by the PMOS FET because NMOS FET PMOS FET can be interchanged.

Allowable Subject Matter

5. Claims 24-29,31 are allowable over the prior art of record because none of these references disclose or can be combined to yield the claimed invention such as PMOS transistor trigger device coupled to the SCR, wherein the drain is coupled to ground and the source is coupled to the trigger tap; the source is coupled to the pad via a shunt resistor; and the pad is further coupled to the protected circuitry as recited in claim 24.

Conclusion

6. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Tan Tran whose telephone number is (703) 305-3362. The examiner can normally be reached on M-F 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization

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where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

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